AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Withdrawn) A method for adapting to specific needs an integrated circuit comprising a stack of insulating layers, each layer being associated with a determined metallization level, metal areas of the last metallization level forming electric contacts of the integrated circuit, comprising the steps of:

(a) forming pairs of metal regions of the penultimate metallization level having a facing edge and connected to components of the integrated circuit;

(b) depositing an insulating layer;

(c) etching according to the specific needs the insulating layer to expose the facing edges of the metal regions of determined pairs; and

(d) forming metal portions of the last metallization level which cover the facing edges of the metal regions of all pairs and which contact the metal regions of the determined pairs.

2. (Withdrawn) The method of claim 1, wherein step (d) comprises depositing a metal layer of the last metallization level, and delimiting in the metal layer said metal portions.

3. (Withdrawn) The method of claim 2, wherein the metal areas are delimited in the metal layer simultaneously with the metal portions.

4. (Withdrawn) The method of claim 3, further comprising:

depositing a passivation layer; and

etching openings exposing the metal areas.

5. (Withdrawn) The method of claim 1, wherein the etching of the insulating layer is a direct etching by an electron beam.

6. (Withdrawn) The method of claim 1, wherein the metal portions are metal connection balls.

7. (Currently amended) An integrated circuit adapted to specific needs, comprising a stack of insulating layers, each layer being associated with a determined metallization level, metal areas of the last metallization level forming electric contacts of the integrated circuit, the integrated circuit comprising:

pairs of metal regions of the penultimate metallization level having a facing edge, and connected to components of the integrated circuit;

insulating portions covering the facing edges of the metal regions of determined pairs according to the specific needs and not covering the facing edges of the metal regions of at least one pair other than the determined pairs~~, the edges of at least one pair of the metal regions not being covered by the insulating portions~~; and

metal portions of the last metallization level which cover the facing edges of the metal regions of all of the pairs of metal regions ~~and which~~, the metal portions connecting the metal regions of the at least one pair [[pairs]] other than the determined pairs and not connecting the metal regions of the determined pairs, [[the]] each of the insulating portions ~~associated with the determined pairs~~ being interposed between the facing ~~metal~~ edges of the metal regions of [[the]] a determined pair [[pairs]] and ~~the associated~~ a covering one of the metal portions ~~of the last metallization layer~~ that is associated with the determined pair.

8. (Original) The integrated circuit of claim 7, further comprising a passivation layer covering the metal portions.

9. (Currently amended) An integrated circuit comprising a stack of insulating layers, each layer being associated with a metallization level, metal areas of an uppermost metallization level forming electric contacts of the integrated circuit, the integrated circuit comprising:

pairs of metal regions of the penultimate metallization level having a facing edge and connected to components of the integrated circuit;

insulating portions covering the facing edges of the metal regions of determined pairs and

not covering the facing edges of the metal regions of at least one pair other than the determined pairs; and

metal portions of the uppermost metallization level which cover the facing edges of the metal regions of all pairs ~~and which~~ , the metal portions connecting ~~, for at least one pair of metal regions,~~ the metal regions of the at least one pair [[pairs]] other than the determined pairs and not connecting the metal regions of the determined pairs.

10. (Previously presented) The integrated circuit of claim 9, further comprising a passivation layer covering the metal portions.

11. (Previously presented) An integrated circuit, comprising:

pairs of metal regions formed in a metallization level and having facing edges;

at least one insulating portion covering the facing edges of at least one first pair of the pairs of metal regions so as to encode at least one first bit ~~having a first polarity~~; and

metal portions that cover the facing edges and connect at least one second pair of the pairs of metal regions so as to encode at least one second bit having an opposite binary value with respect to the first bit ~~having a second polarity~~, the metal portions being formed in an uppermost metallization level of the integrated circuit.

12. (Withdrawn) The integrated circuit of claim 11, wherein the metal portions are metal connection balls.

13. (Previously presented) The integrated circuit of claim 11, further comprising a passivation layer covering the metal portions.

14. (Previously presented) The integrated circuit of claim 11, wherein the integrated circuit is adapted to specific needs.

15. (Previously presented) The integrated circuit of claim 11, wherein the pairs of metal regions are formed in a penultimate metallization level of the integrated circuit.

16. (Previously presented) The integrated circuit of claim 11, wherein the integrated circuit encodes a code having a plurality of bits, each bit being encoded by whether or not a pair of the metal regions is connected.

17. (Previously presented) The integrated circuit of claim 16, wherein the integrated circuit hinders detection of the code by visual methods.